The 19th U.S.-Korea Forum on Nanotechnology Invited Talk

Electro-Thermal Co-Design of High-Power Semiconductor Devices

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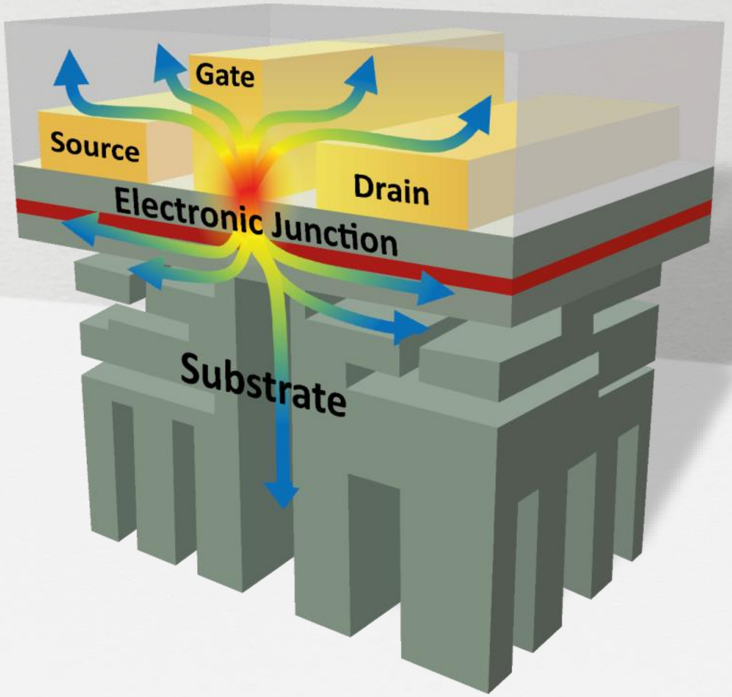
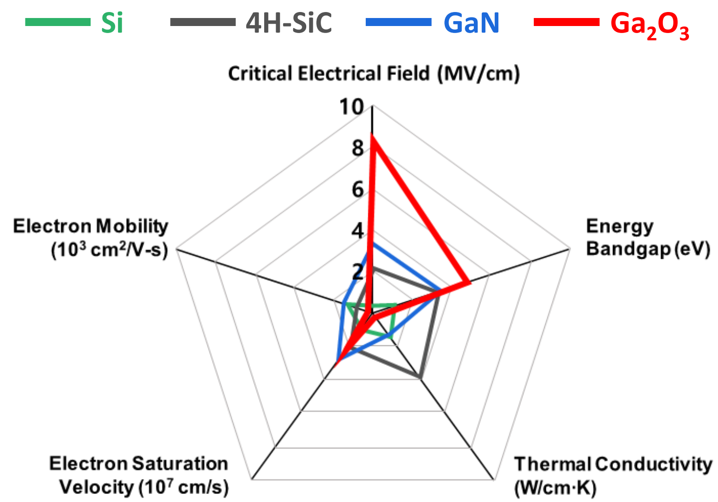
2025. 07. 03

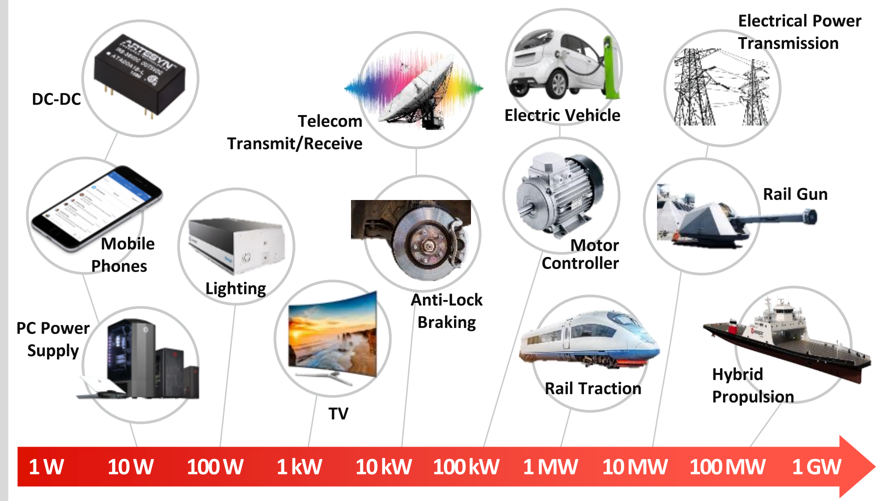


Next-Generation Power Semiconductors: WBG Gallium Nitride (GaN) & UWBG Gallium Oxide (Ga_2O_3)

Outstanding Electrical Properties



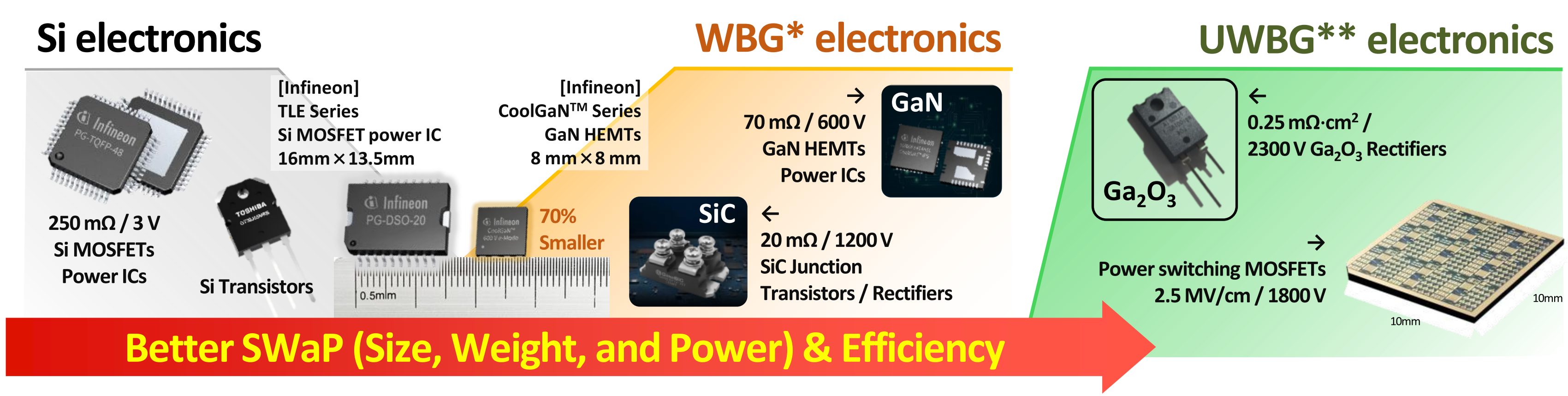
Potential Applications



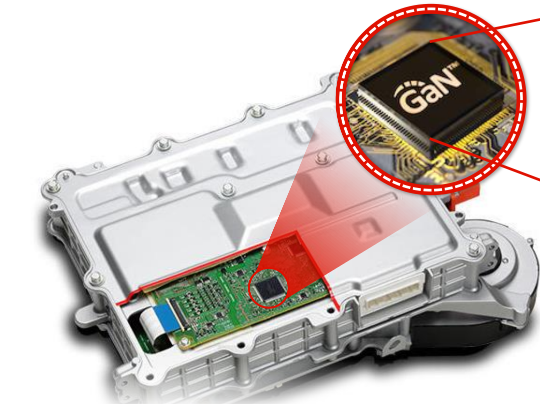
* WBG: Wide Bandgap

** UWBG: Ultrawide Bandgap

Better SWaP and Efficiency

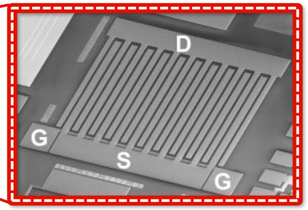


Thermal Challenges in WBG GaN Electronics: Device Self-Heating Limits Electrical Performance

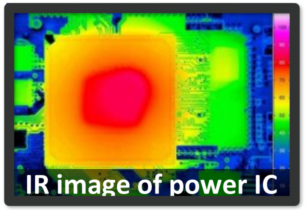


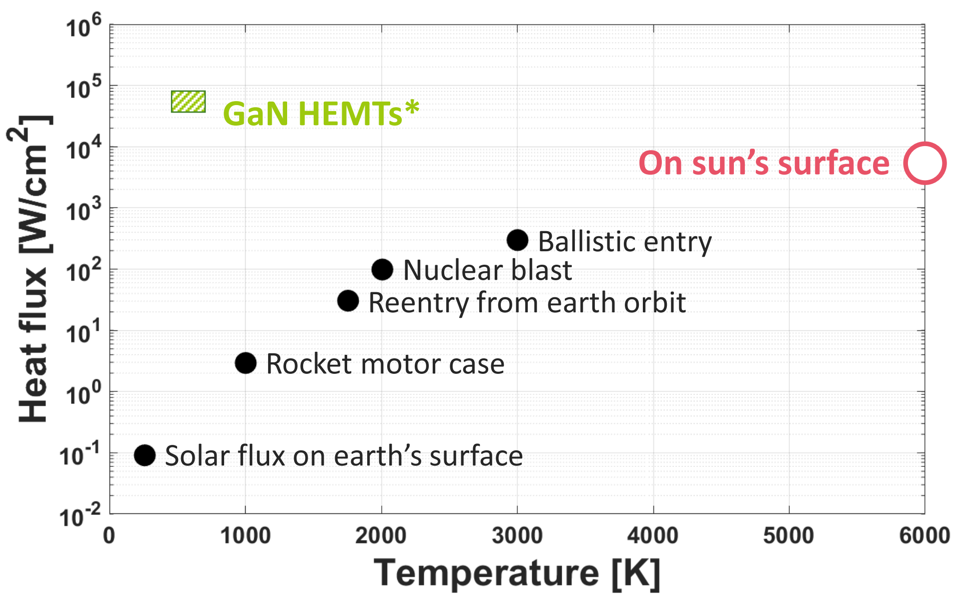
GaN-based EV on-board charger

Toyota Industries Corporation



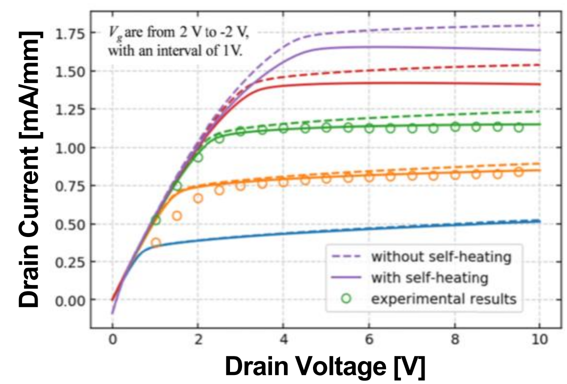
Multi-gate GaN HEMT



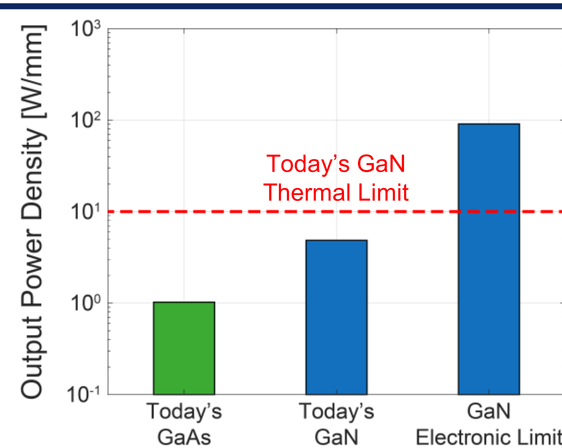


Performance Degradation

Current Droop



Derated Output Power Density



* HEMTs: High-electron-mobility transistors

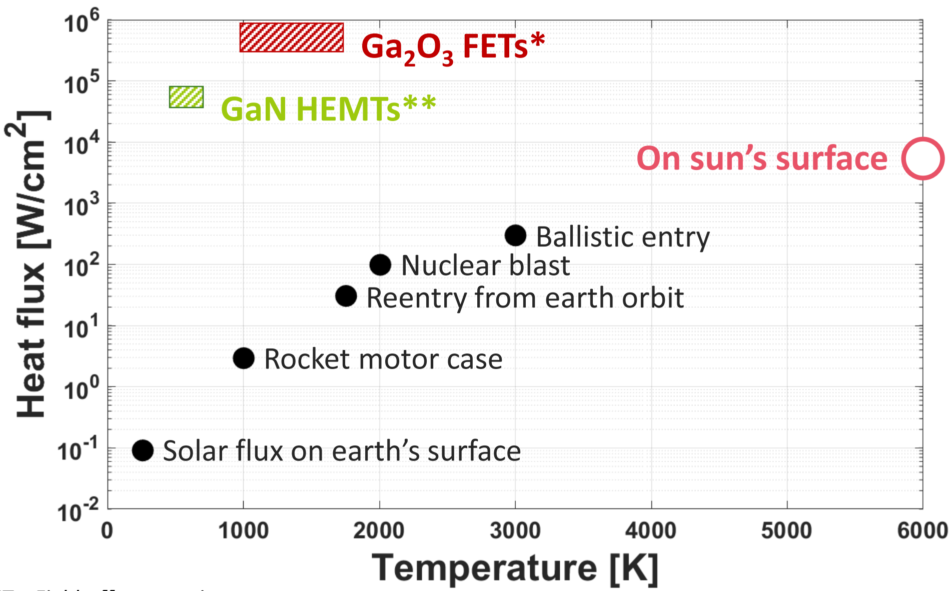
X. Chen et al., IEEE Trans. Electron Devices (2019)
DARPA, HR001123S0013 (THREADS)

Thermal Challenges in UWBG Ga_2O_3 Electronics: Low Thermal Conductivity Aggravates Device Self-Heating

Property	Legacy	WBG		UWBG
	Si	SiC	GaN	Ga_2O_3
Energy Bandgap [eV]	1.1	3.3	3.4	4.8
JFOM* [$v_{sat}E_C$]	1	17	28	29
BFOM** [$\mu\varepsilon E_c^3$]	1	340	870	3400
Thermal Conductivity [W/m/K]	150	270	210	11 - 27

10-20X lower

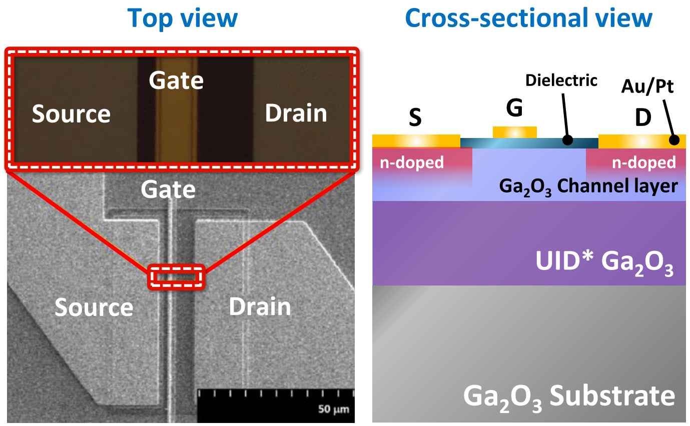
* *JFOM: Johnson's figure of merit*
** *BFOM: Baliga's figure of merit*



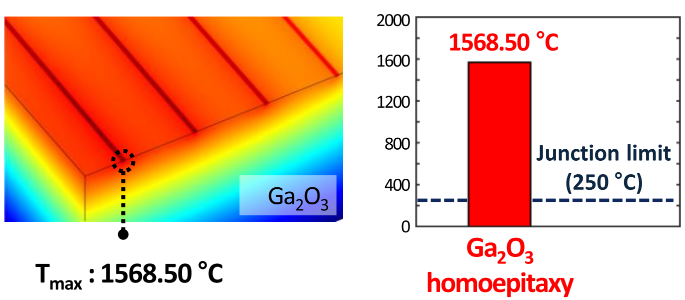
* *FETs: Field-effect transistors*
** *HEMTs: High-electron-mobility transistors*

Device Self-Heating in Homoepitaxial Ga_2O_3 Devices

β-Ga_2O_3 Homo-Epi Device Structure



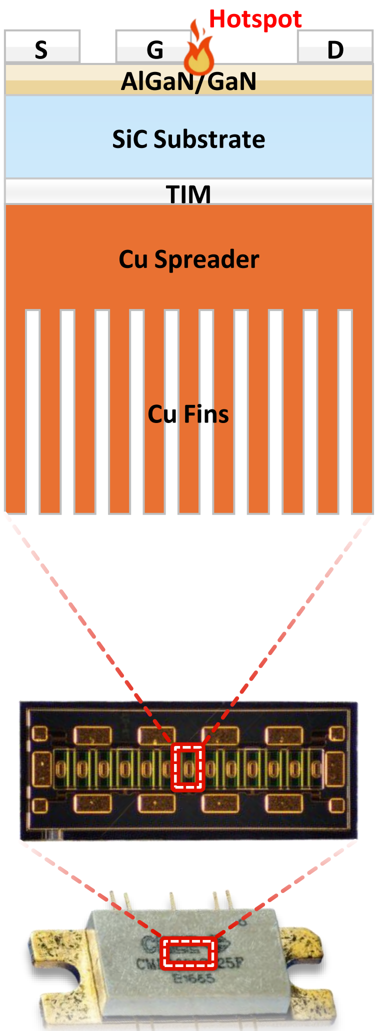
FEM** Device Thermal Modeling



* *UID: Unintentionally-doped* ** *FEM: Finite element method*

H. Dong et al., IEEE Electron Device Letters (2019)
B. Chatterjee et al., IEEE Trans. CPMT (2019)

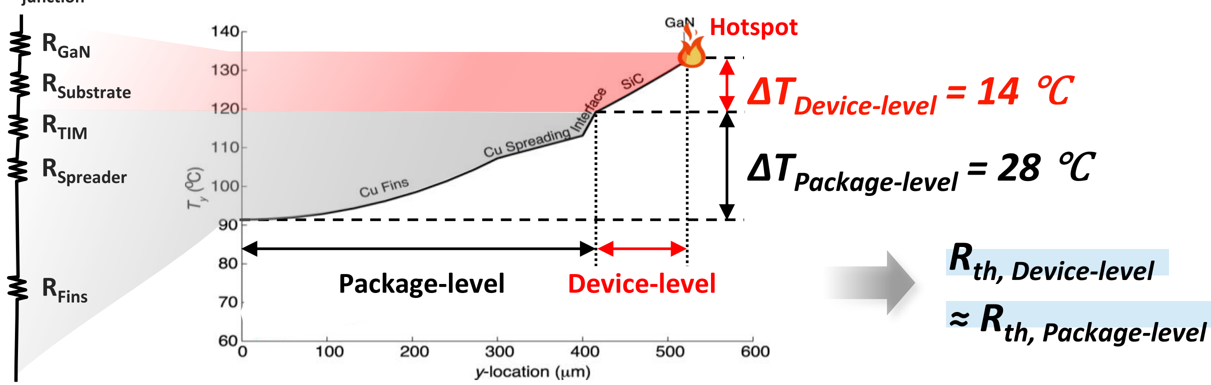
Device Self-Heating Compromises Device Reliability & Long-Term Sustainability



CREE GaN CMPA601C025 Power Amplifier

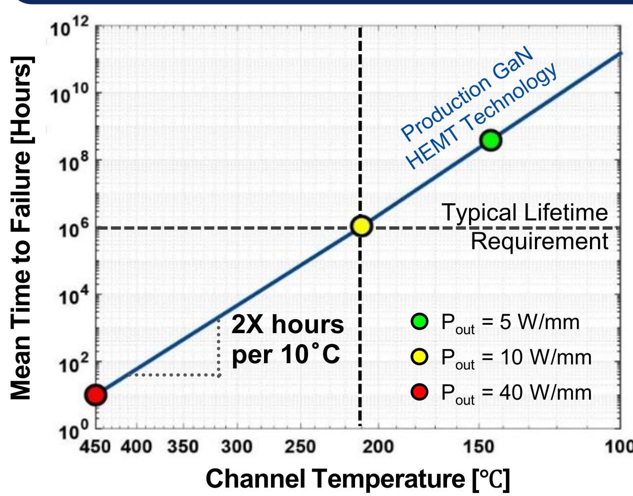
Device-Level vs. Package-Level Temperature Rises

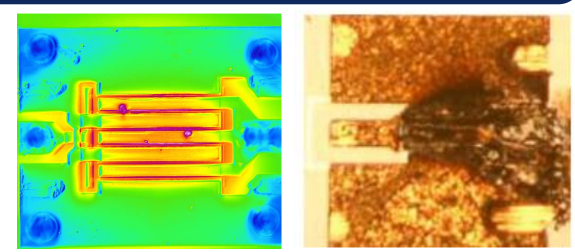
Y. Won, **J. Cho** et al., IEEE Trans. CPMT (2015)



TIM: Thermal interface material *R_{th}: Thermal resistance*

Device Self-Heating Reduces Reliability & Sustainability





For every 10°C rise in channel temperature, device lifetime is reduced by half.

DARPA, HR001123S0013 (THREADS)

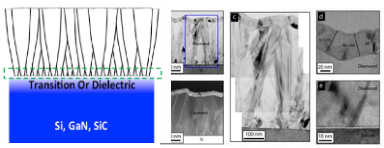
Device-Level Thermal Management Solutions: DARPA Drives NJTT, ICECool, and THREADS…

DARPA NJTT Program ('09-'14)

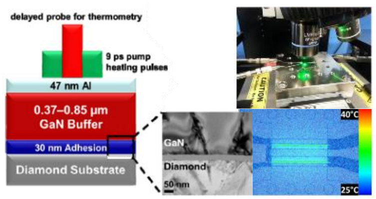
Near-Junction Thermal Transport

Goal: Improve near junction(< 100 μm) thermal transport

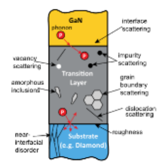
- High Thermal Conductivity Substrate
- Thermophysical Property Measurement
- Removal of Low-k Epitaxial and Transition Layers



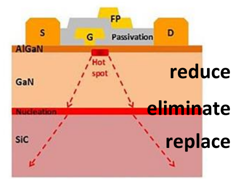
CVD diamond substrate



Thermoreflectance



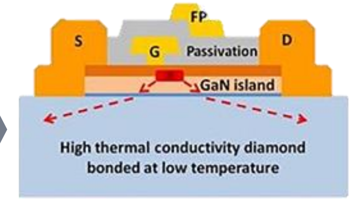
Hetero-interface



Removal of low-k

Device-level Thermal Management

"3× power handling in GaN Power Amplifier"



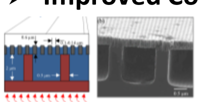
GaN-on-Diamond

DARPA ICECool Program ('12-'14)

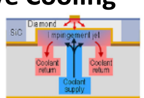
Intrachip/Interchip Enhanced Cooling

Goal: Embedded microfluidic cooling inside substrate (>1kW/cm²)

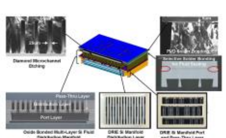
- Improved Convective Cooling



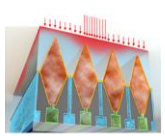
Thin film evaporation



Jet impingement



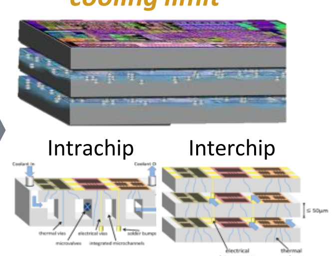
Manifold-microchannel



Hierarchical porous coating w/ phase separation

Integrated Embedded Cooling

"Overcome convection cooling limit"



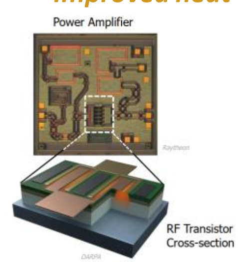
Embedded Cooling

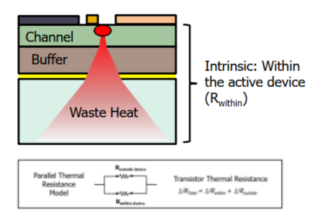
DARPA THREADS Program ('23-'27)

Technologies for Heat Removal in Electronics at the Device Scale

Goal: Robust (MTTF 10^6 hr), High power density (16×)

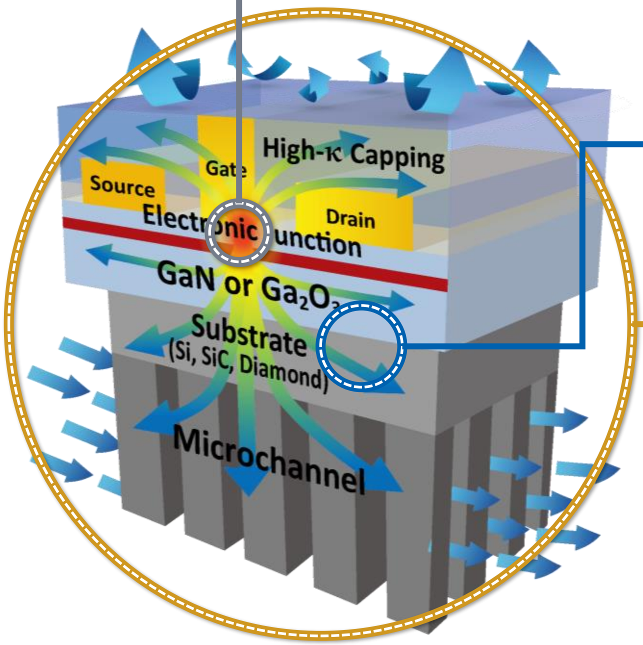
"Improved heat removal at device scale"





THREADS Concepts

Electro-Thermal Co-Design Techniques are Necessary to Overcome Device Overheating & Reliability Concerns



1. Junction temperature measurement

- Device thermal imaging : Sub-μm resolution optical thermography (e.g., Raman, thermoreflectance imaging)

2. Device-level thermal property measurement

- Laser-based pump-probe thermoreflectance
- Epitaxial film thermal conductivity, film/substrate thermal boundary resistance (TBR)

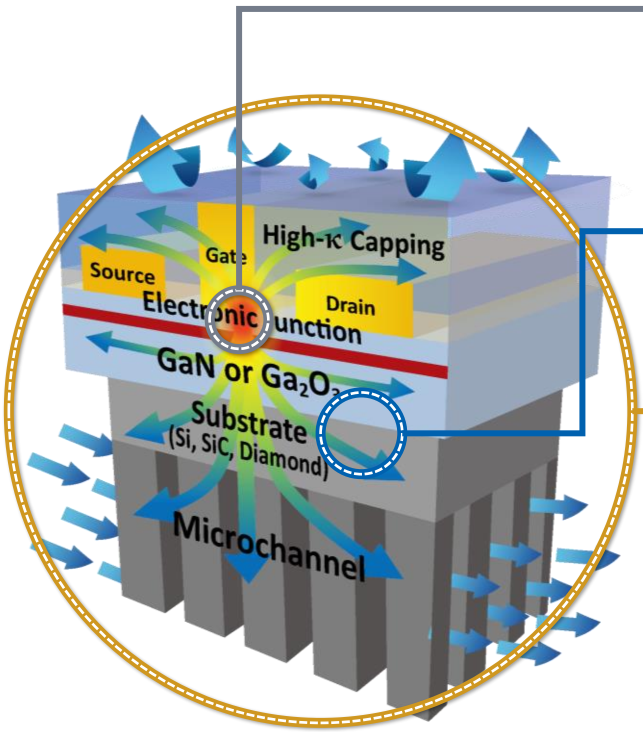
3. Electro-thermal co-modeling

- Thermal/electronic transport
- Energy conversion (heat generation)
- Electrical output characteristics
- Device self-heating behavior

Device-level thermal management solutions

- **Low thermal resistance composite substrate for bottom-side cooling**
- **High thermal conductivity capping overlayer for top-side cooling**
- **Embedded microfluidic cooling close to the heat source**

Electro-Thermal Co-Design:
A *Design for Sustainability* Paradigm



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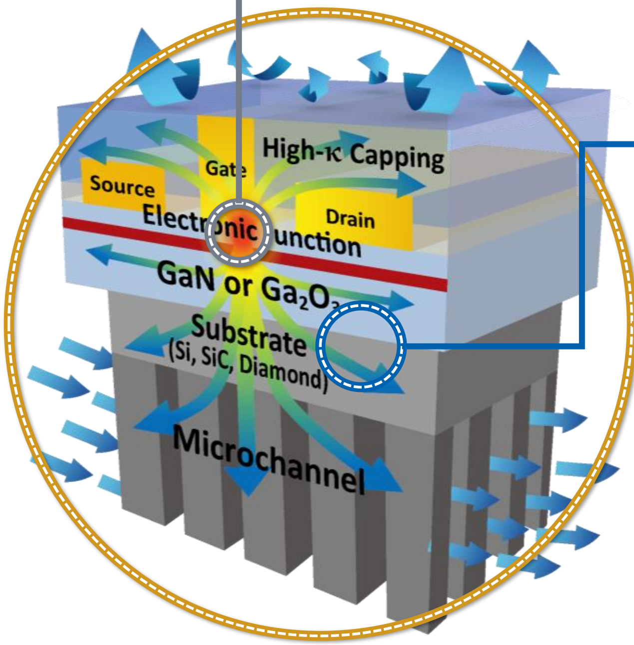

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Key Methodology: Electro-Thermal Co-modeling

Model inputs

- Electrical properties
- Electrical bias (V_{GS}, V_{DS})
- Thermal properties

Applications

- Device layout & Architecture
- Thermal management
- Accelerated lifetime tests

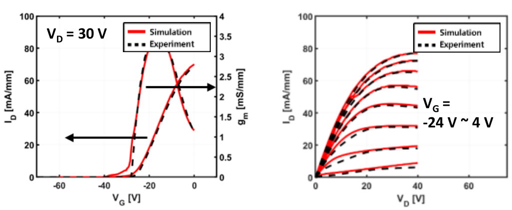
Model outputs

- Electrical output characteristics
- Self-heating behavior

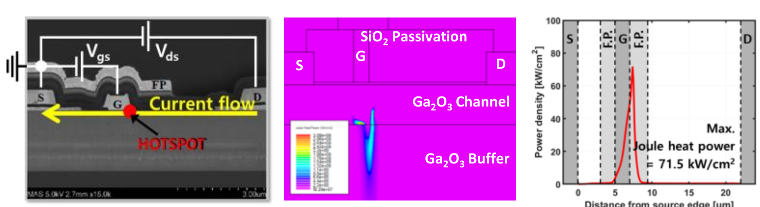
Electrical modeling

Silvaco Atlas

IV characteristics



Heat generation & heat flux profiles

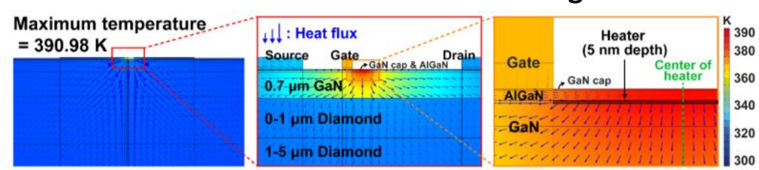


Two-way coupled

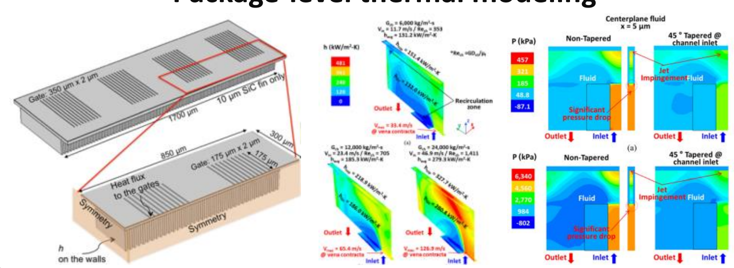
Thermal modeling

COMSOL Multiphysics

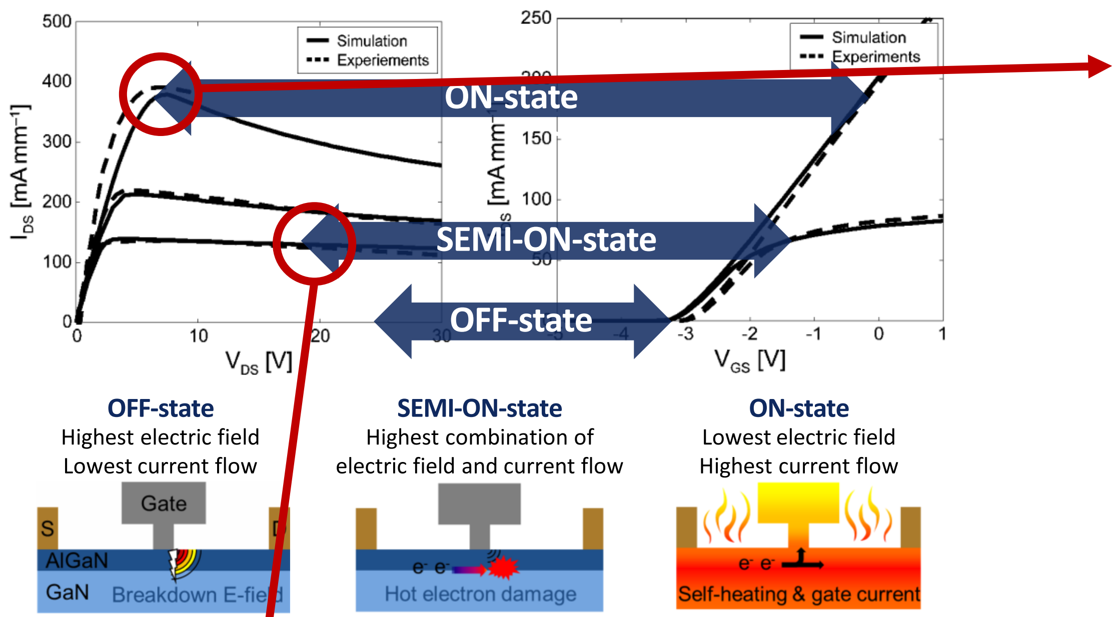
Device-level thermal modeling



Package-level thermal modeling

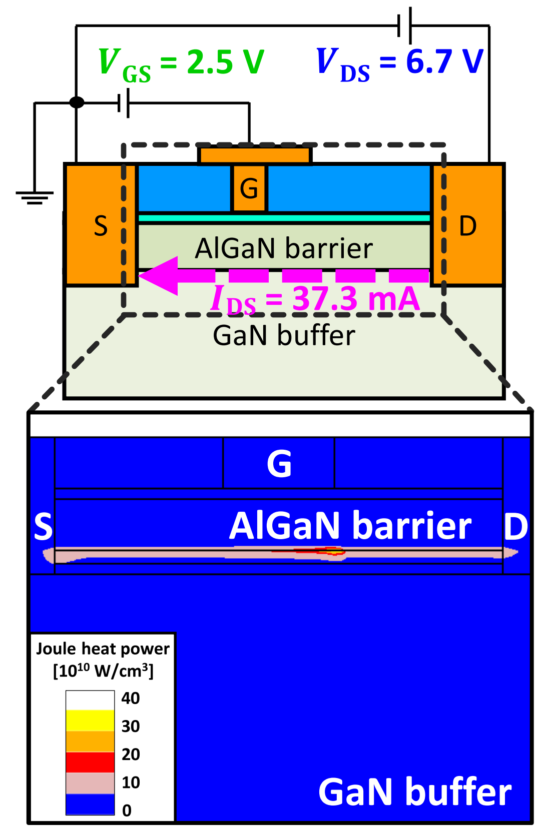


Electrical Modeling of WBG GaN Devices



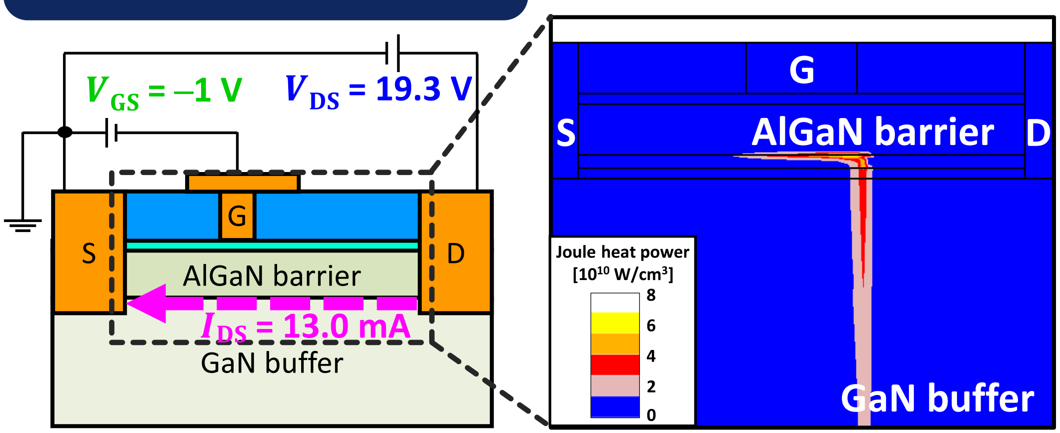
S. Bumham et al., Proceedings of the JEDEC ROCS Workshop (2017)

Fully-open condition



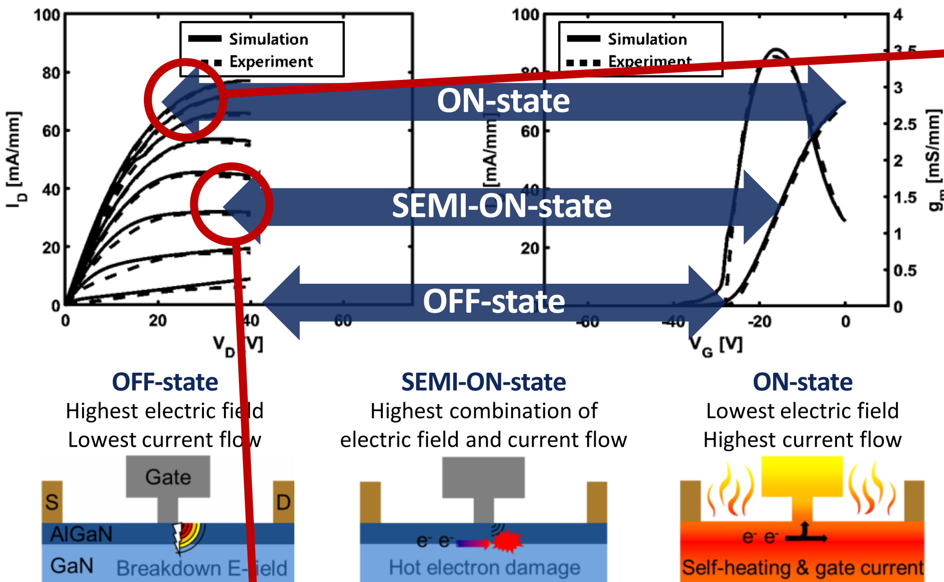
$$P_{DISS} = V_{DS} \times I_{DS} = 250\ mW$$

Pinch-off condition



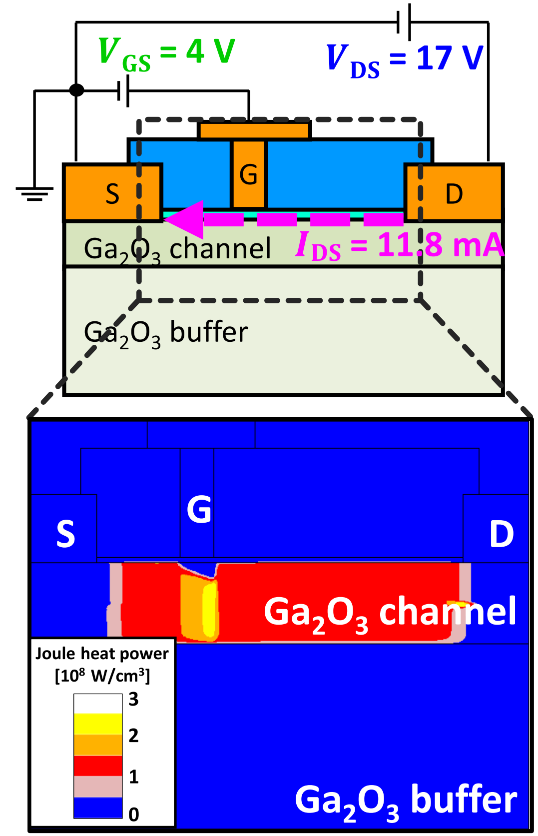
Joule heating profile is a function of applied voltage bias conditions.

Electrical Modeling of UWBG Ga_2O_3 Devices



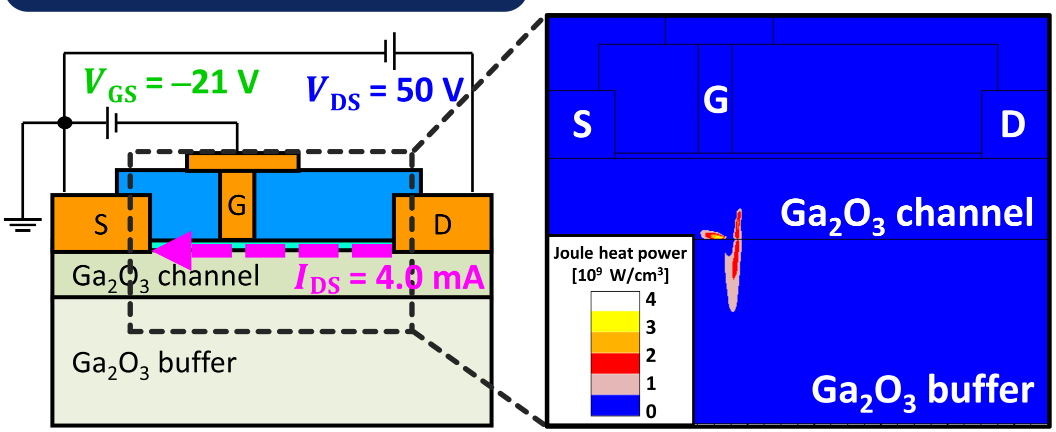
S. Bumham et al., Proceedings of the JEDEC ROCS Workshop (2017)

Fully-open condition



$$P_{DISS} = V_{DS} \times I_{DS} = 200\ mW$$

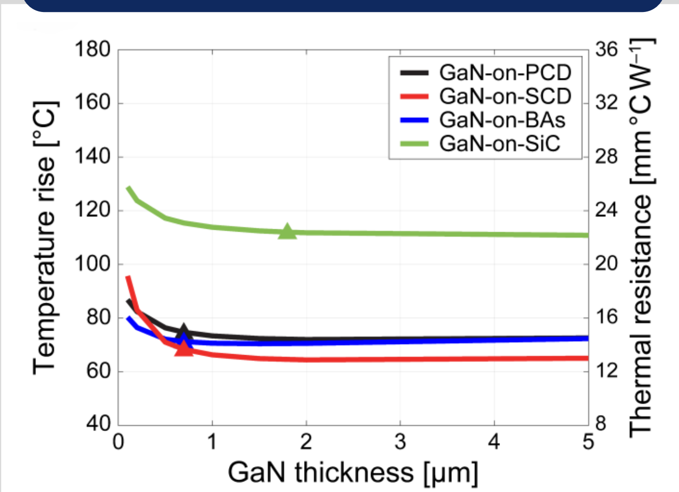
Pinch-off condition

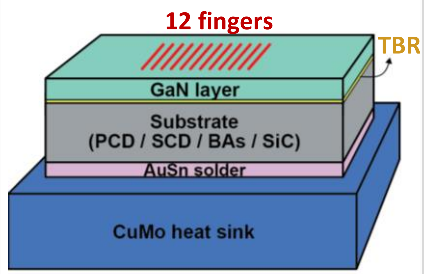


Joule heating profile is a function of applied voltage bias conditions.

Design Considerations for Device-Level Thermal Management of WBG GaN Devices via Substrate Integration

Impact of GaN layer thickness

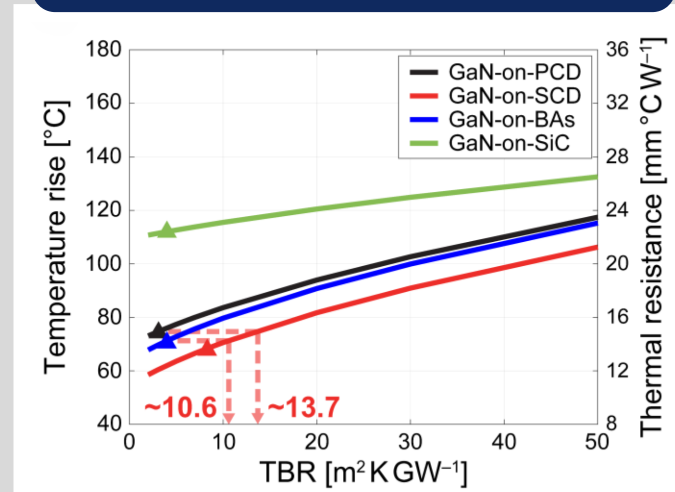




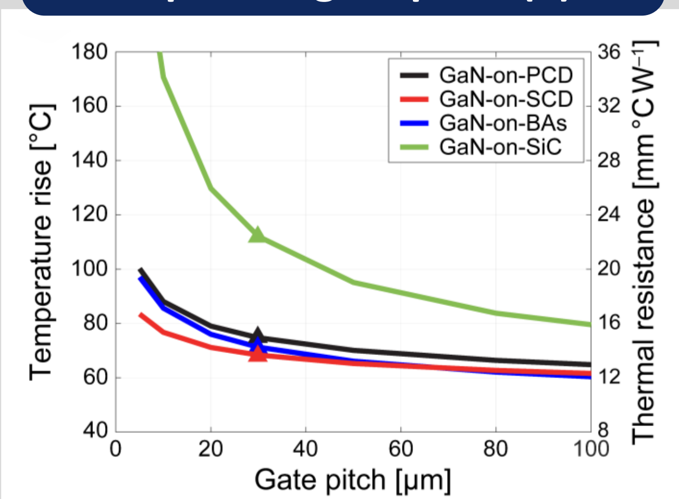
PCD: Polycrystalline diamond

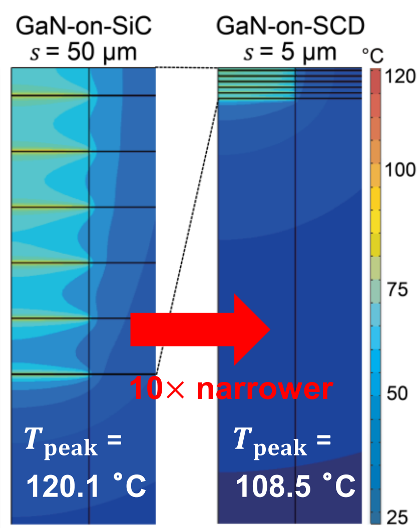
SCD: Single-crystal diamond

Impact of GaN/substrate TBR



Impact of gate pitch (s)

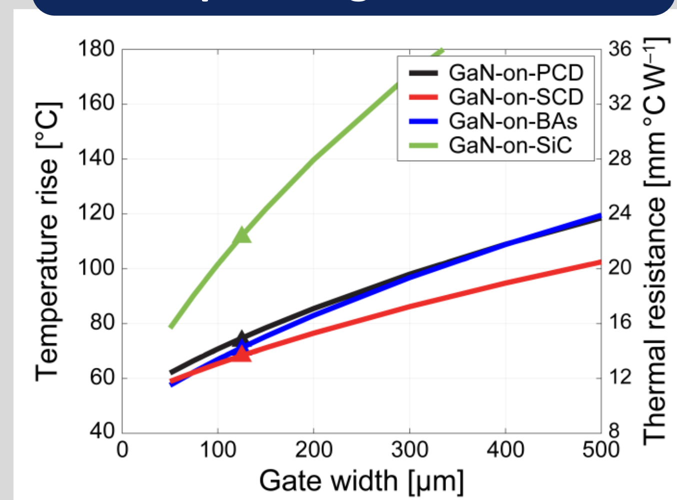




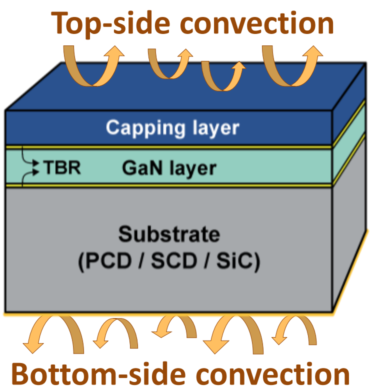
*C. Song, **J. Cho**,* et al. , ICHMT (2023,)*

*C. Song, **J. Cho**,* et al. , under review*

Impact of gate width

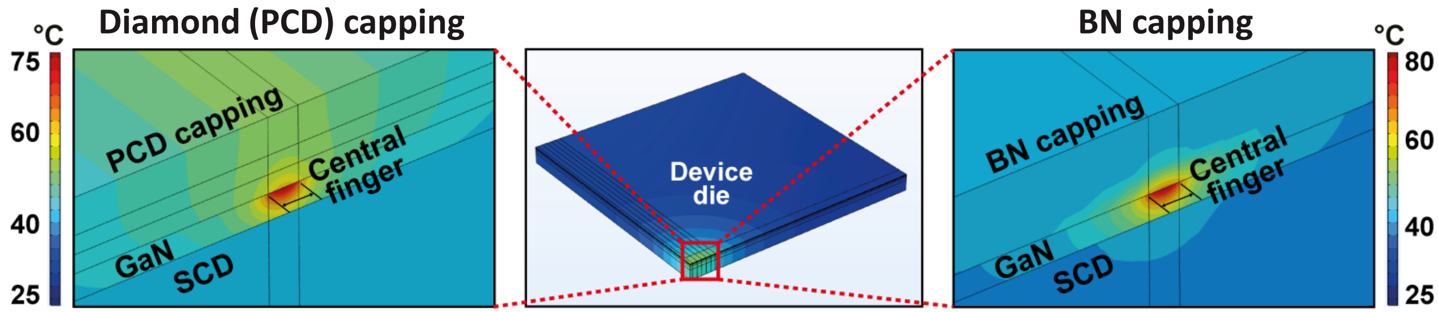


Top-Side Capping Layer can Lower Device Temperatures in WBG GaN Devices



PCD: Polycrystalline diamond

SCD: Single-crystal diamond



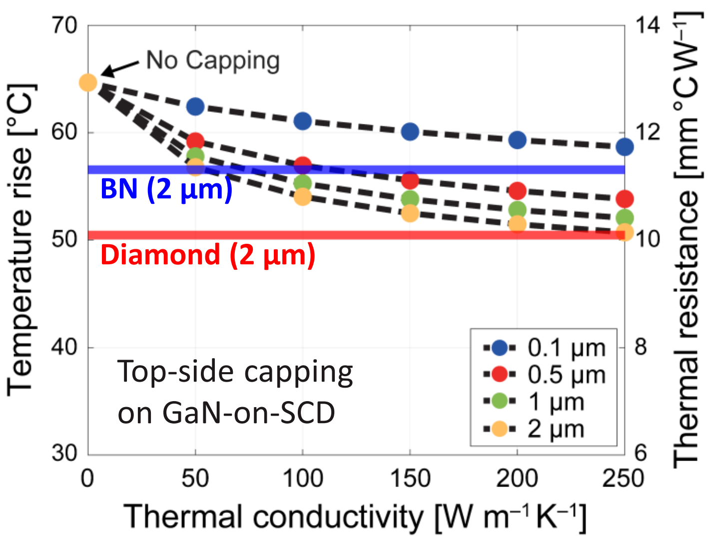
PCD k: Cross-plane = 510 W m^{-1} K^{-1}

(for topmost layer) In-plane = 309 W m^{-1} K^{-1}

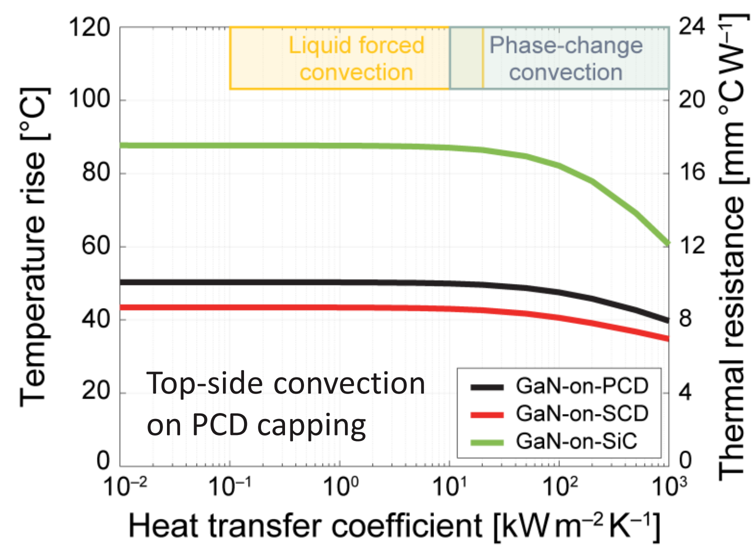
BN k: Cross-plane = 2 W m^{-1} K^{-1}

In-plane = 390 W m^{-1} K^{-1}

Top-Side Conduction Cooling



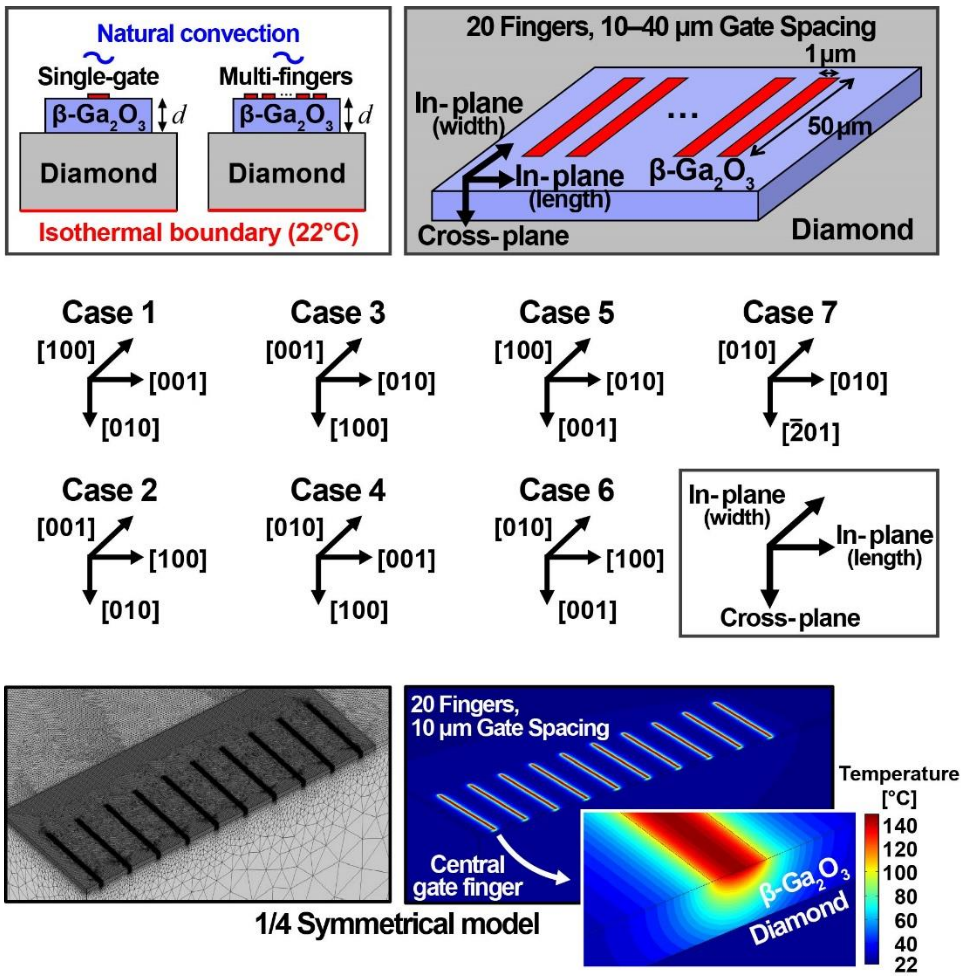
Top-Side Convection Cooling

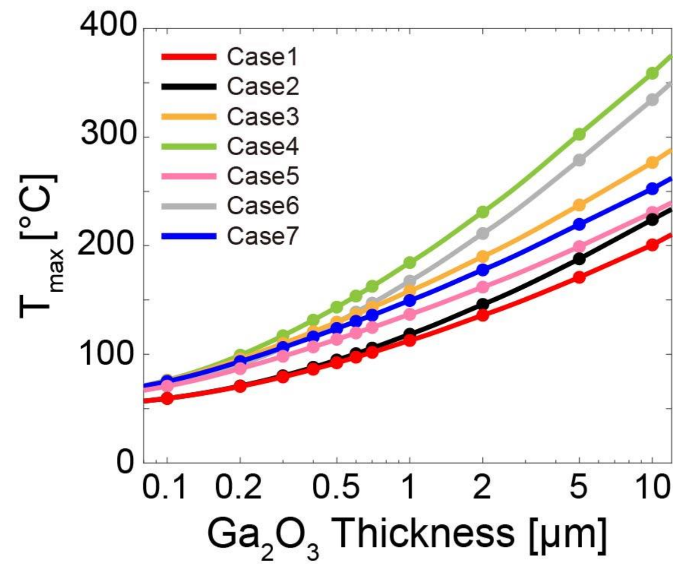


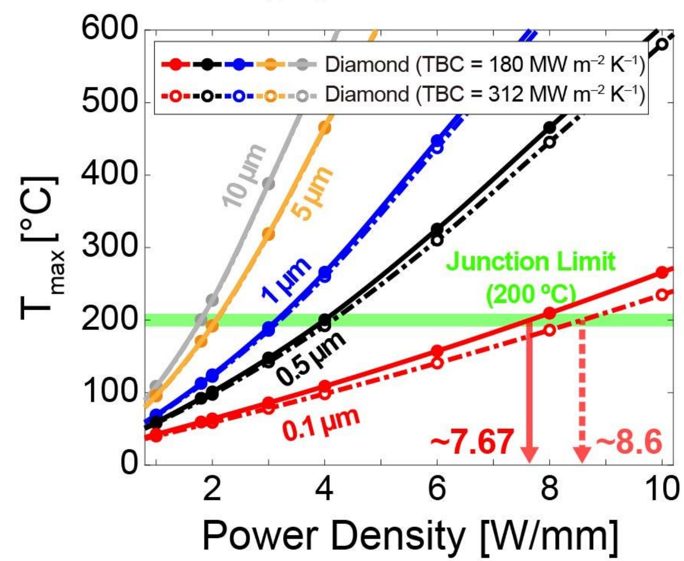
*C. Song, **J. Cho**,* et al. , in preparation*

Impact of Ga_2O_3 Layer Thickness and Anisotropic Thermal Conductivity on Ga_2O_3-on-Diamond Devices

Ga_2O_3-on-diamond Heteroepitaxy Devices

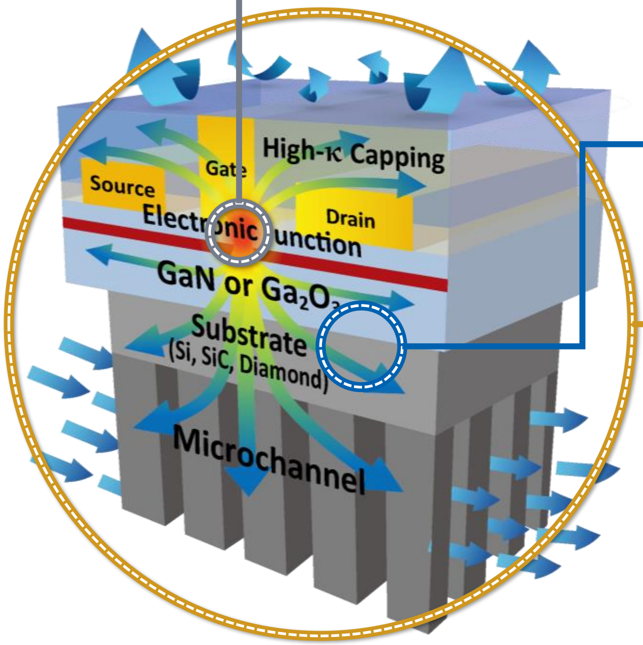






*T. Kim, S. Park, C. Song, H. Lee, and **J. Cho**,* International Journal of Heat and Mass Transfer (2022)*

Electro-Thermal Co-Design: A *Design for Sustainability* Paradigm



1. Junction temperature measurement

- Device thermal imaging : Sub-μm resolution optical thermography (e.g., Raman, thermoreflectance imaging)

2. Device-level thermal property measurement

- Laser-based pump-probe thermoreflectance
- Epitaxial film thermal conductivity, film/substrate thermal boundary resistance (TBR)

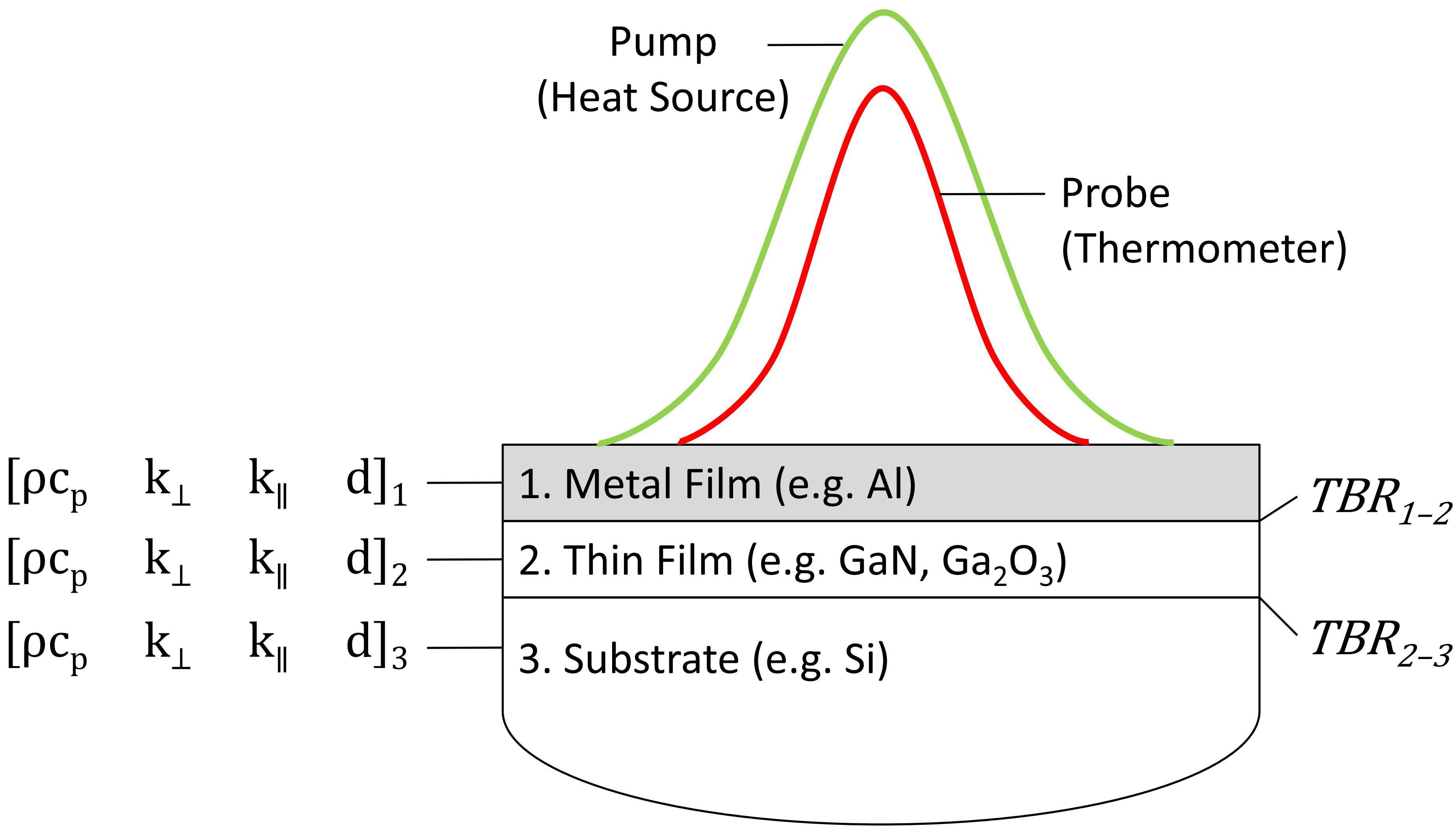
3. Electro-thermal co-modeling

- Thermal/electronic transport
- Energy conversion (heat generation)
- Electrical output characteristics
- Device self-heating behavior

Device-level thermal management solutions

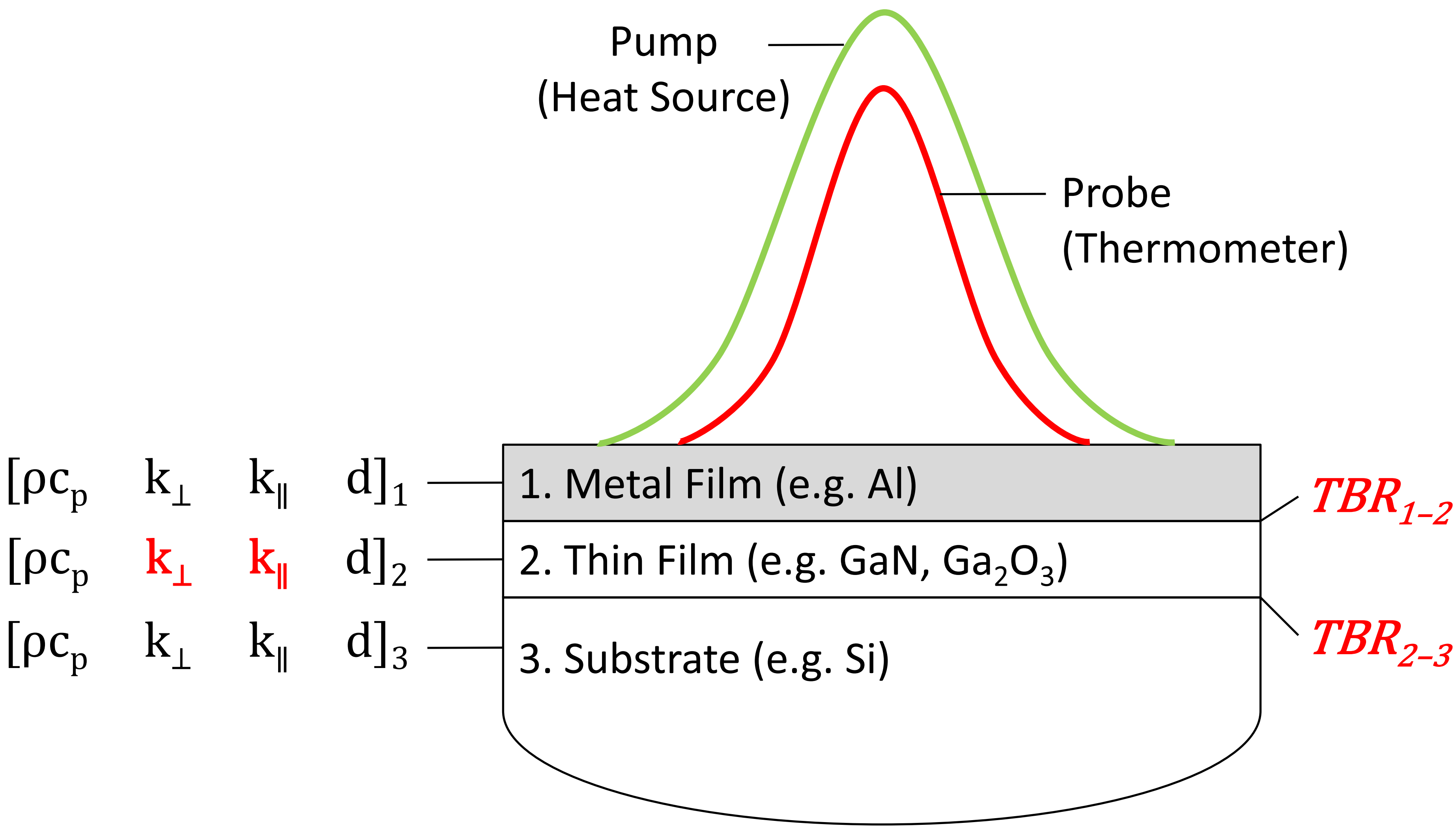
- **Low thermal resistance composite substrate for bottom-side cooling**
- **High thermal conductivity capping overlayer for top-side cooling**
- **Embedded microfluidic cooling close to the heat source**

Key Methodology: Pump-Probe Thermoreflectance



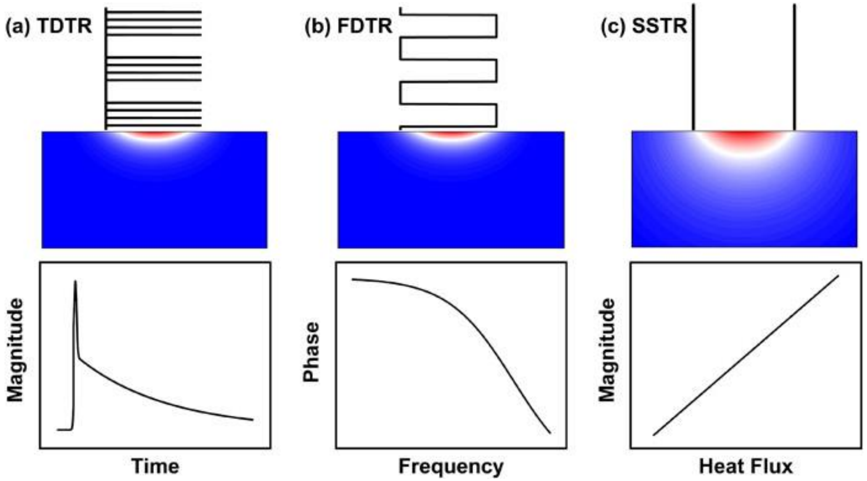
TBR: Thermal Boundary Resistance

Key Methodology: Pump-Probe Thermoreflectance

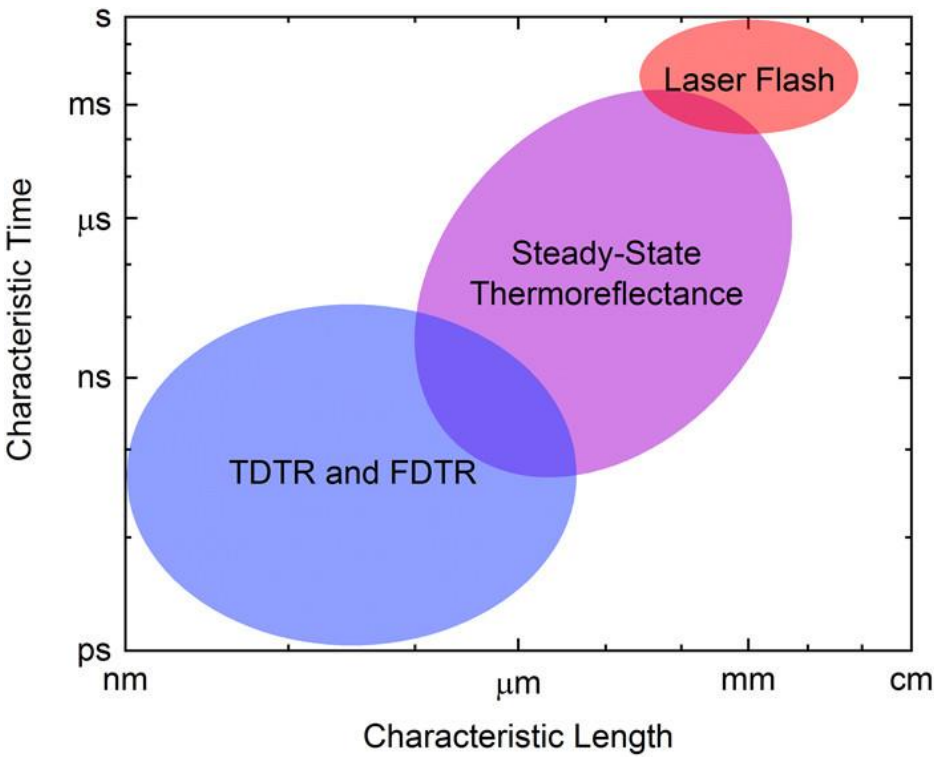


TBR: Thermal Boundary Resistance

Thermoreflectance Regime Map



D.H. Olson, P.E. Hopkins et al, J. Appl. Phys. (2019)

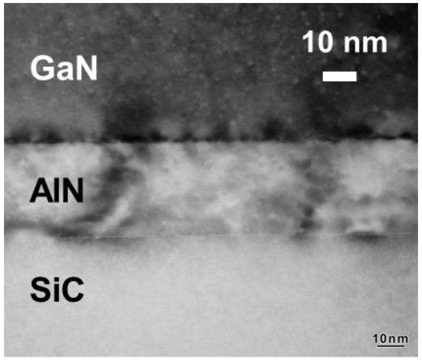


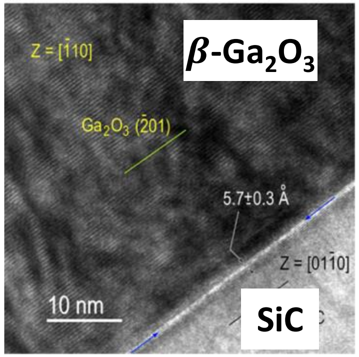
Depth Resolution

- **Time-Domain Thermoreflectance (TDTR)**: a few nm to a few µm
- **Frequency-Domain Thermoreflectance (FDTR)**: a few nm to tens of µm
- **Steady-State Thermoreflectance (SSTR)** : a few µm to tens of µm

Heterogeneous Integration for Power Semiconductors: Heteroepitaxial vs. Bonded Architectures

Heteroepitaxy

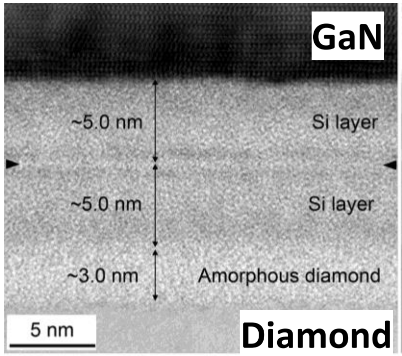


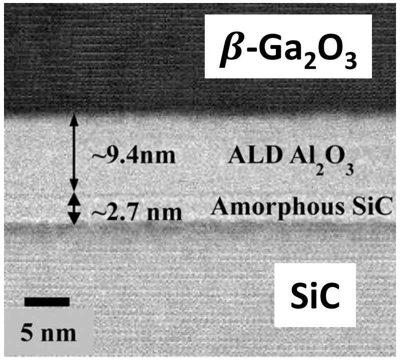


J. Cho, K. E. Goodson et al., PRB (2014)
N. Nepal, S. Graham et al., JVST A (2020)

- Creation of lateral power devices via MOCVD, MBE, HVPE, etc.
- Necessitated by the lack of bulk substrates, particularly for GaN (e.g., GaN-on-Si, GaN-on-SiC)
- Can introduce interfaces with defects and complex interfaces within the device

Bonding





Z. Cheng, S. Graham et al., ACS AMI (2020a)
Z. Cheng, S. Graham et al., ACS AMI (2020b)

- Bonding methods: Surface-activated bonding (SAB), fusion bonding, etc.
- Allows for heterointegration that cannot be performed by heteroepitaxy
- Amorphous adhesive interlayers and interfacial defects can result in high TBR at bonded interfaces

Conclusions

- WBG and UWBG semiconductors hold strong potential for future power and RF electronics, but thermal bottlenecks limit not only device performance but also reliability and long-term sustainability.

- Electro-thermal co-design is essential for mitigating device overheating and improving device reliability.

- Such co-design approaches are central to ‘sustainability by design,’ enabling reduced energy loss, lower cooling costs at the package and system levels, and extended device lifetimes.

- Manufacturing for heterogeneous integration will be a key enabler of future WBG and UWBG technologies, with thermal metrology playing a critical validation role.

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